Effect of Impurities to the Transport Properties of CVD Graphene Cooled with a Biased Gate Voltage

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Electron and hole transport in graphene remains to be a topic of theoretical and experimental interest. In this experimental work, we investigate electron/hole transport in a graphene sample in the form of a Hall bar device, where the graphene was prepared using chemical vapor deposition on copper foils. This study intends to find the result of cooling a graphene specimen under a gate bias on the transport properties. Thus, we present results from the measurements conducted in a liquid nitrogen bath as well as in a closed cycle refrigerator, with a focus on the behavior of the Hall effect under various gate voltages near the charge neutrality point. Further, we study the effect of the gate bias voltage on the charge neutrality point.

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I. INTRODUCTION

Graphene is one of the most popular 2D materials among researchers that triggered many studies. The semimetallic property of graphene which has charge carriers behave like Dirac fermions (zero effective mass)[1], that enables high mobilities up to 200,000 $cm^2V^{-1}s^{-1}$,[2] and many other extraordinary effects. Half-integer quantum Hall effect[3] and ballistic transport properties at room temperature[4] are few examples. Production of high-frequency electronic devices[5] and transparent low resistance conductors[6] will be feasible due to high carrier mobility and lower visible light absorption of graphene.

Obtaining pure graphene is essential and investigating the obstacles for doing that is crucial for the future of nanotechnology. The highest quality graphene with minimum structural defects is achieved by mechanical exfoliation of pyrolytic graphite[7]. However, the exfoliation method can't be utilized in creating large area monolayer graphene. Therefore, a method that can fabricate uniform monolayer graphene in large scale is required. Chemical vapor deposition (CVD) of graphene was demonstrated as an adequate method of growing single-layer graphene[8]. It has been shown that large-area of single-crystal, monolayer graphene (0.5 mm on a side) can be grown with good control, on copper foils[9].

The problem with CVD graphene is the process induced impurities and defects. These Microscopic and macroscopic inhomogeneities results, deviation from ideal graphene. Since graphene is zero bandgap semiconductor, conversion of dominant carrier type can be induced using a gate bias. The conversion from holes to electrons happens without crossing a bandgap[10]. Having the Fermi level at the Dirac point would mean there is no net carrier density. Therefore, one can expect diverging Hall resistance and diagonal resistivity. However, recent experimental observations suggest that holes and electrons undergo an ambipolar transport over a wide range of gate voltage near the charge neutrality point(CNP) of CVD monolayer graphene[11]. This observation was explained by the formation of electron-hole streams[11] or puddles[12] at the Dirac point, that arise due to impurities or graphene ripples[13].

A. Possible impurities involved with CVD graphene

Graphene transferred on to silicon dioxide substrates are found to be p-type in most cases due to doping by unintentional adsorbates[14]. At ambient conditions, molecules like water and oxygen can interact with the underline substrate since the graphene is only a single atomic layer. Once the sample exposed to ambient conditions, the doping state remains unchanged even in a vacuum.

The traditional wet transfer method use to transfer graphene grown on copper to the substrate can leave metal ions such as Cu^{2+} and Fe^{3+} trapped between the graphene layer and the substrate. The copper layer is typically etched by oxident solutions such as iron (III) nitrate[15], iron (III) chloride[16] and then cleaned by distilled water. Even after cleaning several times, there can be Fe^{3+} ions that could contaminate the graphene[17].

B. Effect of impurities to the carrier transport

Impurities influence the transport properties of graphene through several mechanisms. Adsorbed water molecules will act as dipoles that oriented randomly. In an applied electric field, these dipoles will align them self along the electric field direction which will create a capacitive gating effect locally[14].

Silicon dioxide formes silanol bonds on its surface at ambient conditions. Oxygen and water molecules that are close to the graphene SiO_2 interface will undergo a

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chemical redox reaction by trapping electrons and de-trapping electrons based on the polarity of the applied electric field (Gate bias)[14].

Ions that are trapped in the interface can drift through the SiO_2 at higher temperatures[18]. The movement of these ions will vary the distance to the graphene layer leading to a change in the localized gating effect. The combination of localized gating and charge trapping de-traping effects emerge as the hysteresis in CVD graphene samples.

Here we investigate the influence of impurities on the hysteresis effect and carrier transport of graphene specimen grown by standard CVD method. Further, we demonstrate that the charge neutrality gate voltage can be controlled by cooling the sample with a gate bias.

II. EXPERIMENTAL METHOD

The monolayer graphene was grown on 25μm copper foils by chemical vapor deposition using methane and hydrogen mixture as carbon precursor at about 1000°Celsius[8]. The graphene was transferred onto a 500μm p-doped silicon wafer(100) with 285nm of oxide layer using conventional wet transfer method[16]. Here we used millimeter-scale Hall bar devices with p-doped silicon back gate in the configuration depicted as in Fig. 1.

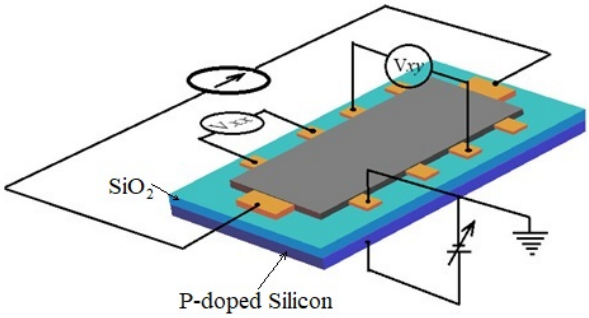

FIG. 1. Schematic of the measurement setup.

A closed cycle refrigerator was utilized for the first part of the experiment that we studied the temperature dependence of the gate hysteresis effect. We were able to cool the system to 15K within four hours. A Sweep rate of 0.5 V/s was used to sweep the back gate voltage. 10μA DC was supplied to the sample, and the Hall and diagonal voltages were measured using digital multimeters.

The influence of the biased gate voltage toward the CNP was studied in a liquid nitrogen cryostat. We used this system due to the fast cooling and heating capability that is convenient for several consecutive cooling cycles. The sample was kept under a specific DC bias about an hour before each cooldown. Once the system reached its base temperature of 78K, Hall and diagonal voltages were measured changing the gate voltage. Nitrogen gas was used as the exchange gas during the cooling and heating process.

III. RESULTS AND DISCUSSION

We measured the hysteresis of our hall bar devices at room temperature first. All of the graphene devices studied, produced reproducible diagonal resistance(R_{xx}) versus gate voltage V_G characteristics in ambient conditions. A representative example is given in Fig. 2(a). The blue and red curves depict the forward and backward sweeping of the gate voltage between -50V and +80V. The CNP shifted about 40V to the positive side of gate voltage, where we define the CNP as the voltage of the back gate at the maximum diagonal resistance point.

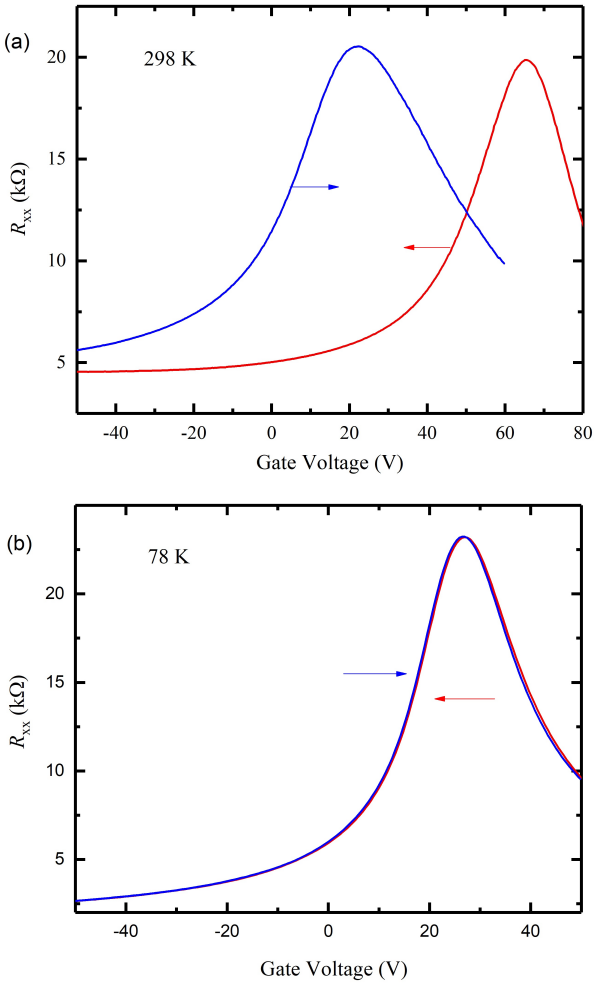

FIG. 2. The diagonal resistance of the graphene sample against the back-gate voltage swept from (a) -50to +80V at a temperature of 298K,(b) -50V to +50V at a temperature of 78K. Forward and backward sweeps were indicated by blue and red curves respectively.

The hysteresis we observed here can be explained by charge trapping and de-trapping at the SiO_2-graphene

interface and the top surface of graphene. When we are at a positive gate voltage, the electron concentration on graphene is higher compared to the holes. Traping centers will trap electrons and reduce the effective electron concentration on graphene. This will reduce the effective gate voltage moving the CNP to a more positive voltage. Similarly, the effect of a negative gate voltage can be explained as trapping and de-trapping of holes. Trapped charges will remain trapped until the polarity of the gate is switched. Silicon dioxide has silanol groups on the surface that act as charge traps. Thermally grown SiO_2 has effective trap density about 5×10^{10} cm^{-2} interface traps and about 5×10^{11} cm^{-2} oxide traps[14].

We observed a reduction of hysteresis with reduced temperature. The Fig. 2 (b) shows that there was no significant shift in CNP at the temperature of 78K when comparing forward and backward sweeps represented in blue and red colors respectively. Hysteresis depends on the sweep rate as well. Therefore we used the data we collected at the rate of 0.5 V/s for our comparison. However, we swept the gate voltage at different speeds like 0.1, 0.8 V/s and also at lower temperatures till 15K which did not provide any evidence of hysteresis (Data not shown here). This may be due to the prolonged time constant of charge trapping and de-trapping mechanism at lower temperatures.

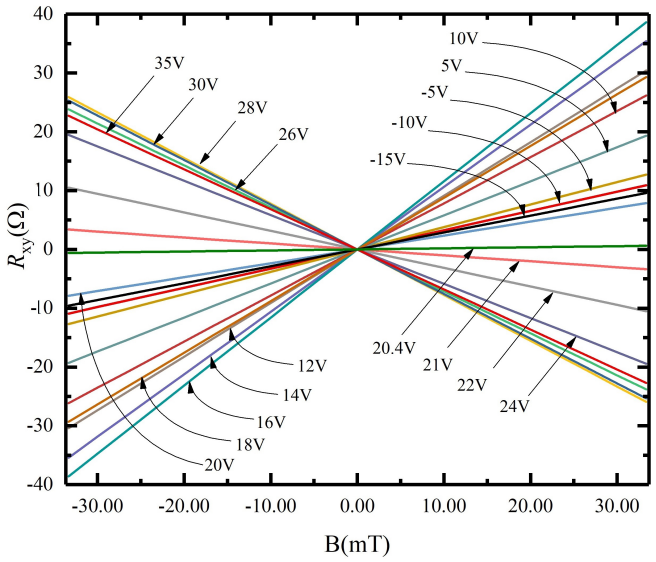

FIG. 3. The Hall resistance of the graphene sample against the magnetic field from -33mT to +33mT at a temperature of 15K with different gate bias near the charge neutrality point of the device. Related gate bias voltages are indicated in black arrows.

Since there was no hysteresis at our base temperature (15K), We were able to study the magnetotransport near the neutrality point without having the neutrality point shifted with the gate bias. Fig. 3 presents the Hall resistance at different gate biases against the magnetic field at a temperature of 15K. We observed our CNP is shifted toward positive V_G, which means there were extra holes in our sampledue to impurities and defects. When we increase V_G, the electron concentration on our sample increases compensating the extra holes leading to a neutral net charge at CNP. Therefore, a positive Hall coefficient is expected in the region before CNP and a negative Hall coefficient afterward. Here the slope of R_{xy} versus $\mathbf{B}$ is positive and increases up to 16 V. From $16 \leq V_G \leq 20.4$ V the slope remains positive while decreasing in magnitude with increasing V_G. The slope is close to zero at V_G=20.4V (vanishing Hall effect). After this point, the slope became negative and increased in magnitude until the V_G reaches to 26V and then started to decrease. The change of sign in the slope we observed here indicate that carrier type contributing to the transport changed from holes to electrons. The vanishing Hall resistance (instead of diverging) can be attributed to the global effect on Hall voltage due to the oppositely directed hall and electron current domains caused by localized impurities[11].

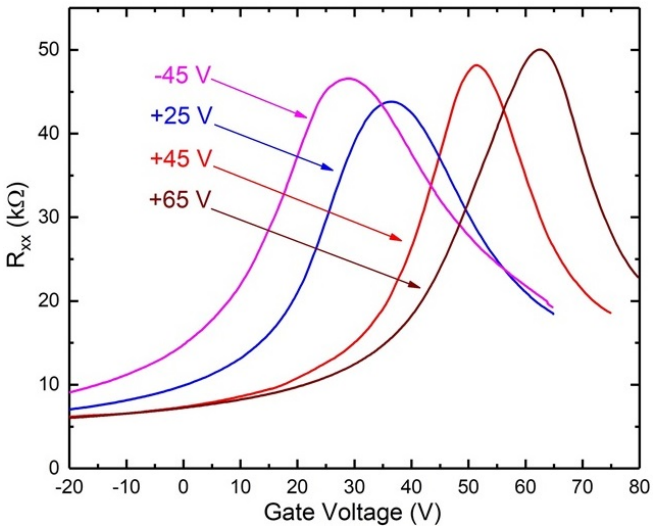

FIG. 4. The diagonal resistance of the graphene sample against the back-gate voltage swept from -20 to +80V at a temperature of 78K cooled with different gate bias applied at room temperature. Related gate bias voltages are indicated in arrows.

Since the CNP changes in a large range at room temperature and stays constant at cryogenic temperatures, we studied the capability of controlling the V_G that charge neutrality occurs by a biased gate voltage supplied during sample cool down from room temperature. We observed the CNP could be easily shifted toward the higher positive V_G side with a positive bias. With a negative V_G bias, we were able to get the CNP shifted toward lower positive V_G, but not to the negative V_G where the device becomes n-type. Here we demonstrate a sample of our results in Fig. 4. The magenta curve is obtained by supplying a bias of -45V and the neutrality point was observed around V_G=27V. With a bias of +25V, the CNP shifted to V_G=36V (blue curve). With +45V and

+65V bias, the CNP shifted further to G_V=52V (red) and G_V=63V (brown) respectively. This observation is evident for the capability of changing the CNP with a biased back gate voltage and keeping it at a specific V_G at cryogenic ($\leq 78K$) temperatures. However, a more systematic study is necessary to reveal the mechanism behind our observation.

IV. CONCLUSION

The hysteretic and electrical properties of back-gated graphene Hall bar devices prepared by standard CVD method were investigated by varying the back gate voltage and the magnetic field perpendicular to the sample at room temperature as well as at cryogenic temperatures. A significant reduction of hysteresis was observed with cooling the device. The hysteresis effect can be explained as a result of the capacitive gating effect that can occur due to localized impurity potentials and the charge trapping and de-trapping mechanism near graphene top and bottom surfaces. The influence of gate sweeping toward impurity potentials got decreased significantly at lower temperatures($\leq$78K). The ability to control the CNP we get at 15K by changing the applied back-gate bias at room temperature is demonstrated.

We found our samples were always p-type. The CNP shift toward positive V_G with a positive gate bias we observed suggest that the charge trapping de-trapping is dominant over the capacitive gating in our samples. The reason is, a capacitive gating will shift the CNP toward the negative V_G direction (to lower positive V_G while sweeping toward higher back gate voltages) which is opposite to what we observed. The charge trapping mechanism agrees with our results, and we believe exposure to ambient conditions have a huge impact on the transport characteristics of CVD graphene. More controlled experiments such as current annealing the sample, changing the sample environment with different gases can be performed to study these effects separately.

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[1] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, Rev. Mod. Phys. **81**, 109 (2009).
[2] J.-H. Chen, C. Jang, X. Shudong, M. Ishigami, and M. S. Fuhrer, Nat. Nanotechnol. **3**, 206 (2008).
[3] X. Du, I. Skachko, F. Duerr, A. Luican, and E. Y. Andrei, Nature **462**, 192 (2009).
[4] X. Du, I. Skachko, A. Barker, and E. Y. Andrei, Nat. Nanotechnol. **3**, 491 (2008).
[5] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, Science **327**, 662 (2010).
[6] R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N. M. R. Peres, and A. K. Geim, Science **320**, 1308 (2008).
[7] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666 (2004).
[8] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, Science **324**, 1312 (2009).
[9] X. Li, C. W. Magnuson, A. Venugopal, R. M. Tromp, J. B. Hannon, E. M. Vogel, L. Colombo, and R. S. Ruoff, Journal of the American Chemical Society **133**, 2816 (2011).
[10] N. H. Shon and T. Ando, Journal of the Physical Society of Japan **67**, 2421 (1998).
[11] R. G. Mani, Applied Physics Letters **108**, 033507 (2016).
[12] J. Martin, N. Akerman, T. Ulbricht, G.and Lohmann, J. H. Smet, K. von Klitzing, and A. Yacoby, Nat. Phys. **4**, 144 (2008).
[13] M. Katsnelson and A. Geim, Philosophical Transactions of the Royal Society of London A: Mathematical, Physical and Engineering Sciences **366**, 195 (2008).
[14] H. Wang, Y. Wu, C. Cong, J. Shang, and T. Yu, ACS Nano **4**, 7221 (2010).
[15] X. Li, Y. Zhu, W. Cai, M. Borysiak, B. Han, D. Chen, R. D. Piner, L. Colombo, and R. S. Ruoff, Nano Letters **9**, 4359 (2009).
[16] K. Yan, H. Peng, Y. Zhou, H. Li, and Z. Liu, Nano Letters **11**, 1106 (2011).
[17] S. Bhaviripudi, X. Jia, M. S. Dresselhaus, and J. Kong, Nano Letters **10**, 4128 (2010), pMID: 20812667.
[18] J. E. Furneaux and T. L. Reinecke, Phys. Rev. B **33**, 6897 (1986).